Course Profile
UVM-RAL

CVC Pvt. Ltd.

VTD Square, 2nd Floor, 183/3 Sarjapura Road, Dommasandra, Bangalore – 562125.
Ph. No. +91-9620209226 +91-9620209223 http://www.cvcblr.com, info@cvcblr.com

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Course Profile

1. UVM RAL - Registers

CVC's UVM-RAL course gives you an in-depth introduction to the register modelling with UVM-RAL. UVM-RAL training gets the user up-to speed with which one can start verifying blocks, IPs, sub-systems and SoCs with large number of configurable registers given a ready-to-use verification environment in UVM. Being an advanced course in UVM, attendees are expected to be fully conversant with Basic UVM and can build IP level testbenches with UVM framework.

2. Class Details:

- Duration: 2-days full time (Can also customize it to 1-day with less topics)
- Prerequisites: Verification, SystemVerilog, UVM (Level-1, to the level of UVC building)
- Enrolling for a class: Please refer to Registration section.

3. Trainers Profiles

Srinivasan Venkataramanan, CTO

http://www.linkedin.com/in/svenka3

- Over 18+ years of experience in VLSI Design & Verification
- Designed, verified and lead several multi-million ASICs in image processing, networking and communication domain
- Worked at **Philips, Intel,** and **Synopsys** in various capacities. Co-authored leading books in the Verification domain.
- Presented papers, tutorials in various conferences, publications and avenues.
- Conducted workshops and trainings on PSL, SVA, SV, VMM, E, ABV, CDV and OOP for Verification
- Holds M.Tech in VLSI Design from prestigious IIT, Delhi.

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Ajeetha Kumari, CEO & MD

http://www.linkedin.com/in/ajeetha

- Has 17+ years of experience in Verification
- Implemented, architected several verification environments for block & subsystems
- Co-authored leading books in the Verification domain.
- Presented papers, tutorials in various conferences, publications and avenues.
- Has worked with all leading edge simulators and formal verification (Model Checking) tools.
- Conducted workshops and trainings on PSL, SVA, SV, OVM, E, ABV, CDV and OOP for Verification
- Holds M.S.E.E. from prestigious IIT, Madras.

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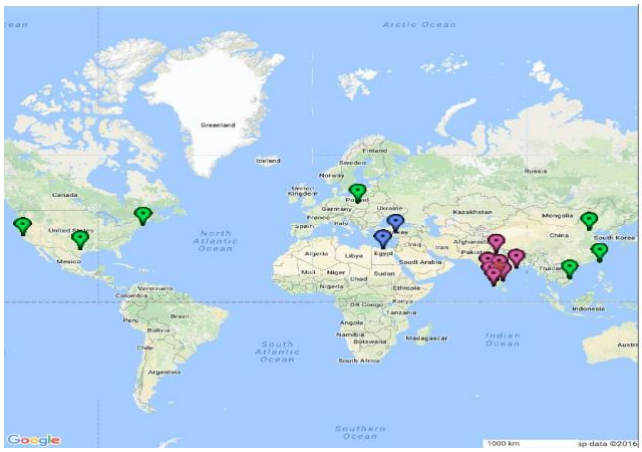
4. Why CVC?

Vendor / Factor	CVC	XYZ training company	EDA Vendor
Training Delivery	World renowned experts	Part timers, in bet'n job engineers	Tool support Engineer
Focus	Verification	Language	EDA tools
Topics covered	User/Verification perspective	Language perspective	Based on the tools strength
How Recently Updated	Last week	Months Back	As old as language was standardized
Verification Expertise	Yes	Depends on the trainer	No
Can I run labs across tools	Yes	Yes	No
Is Content Tool independent	Yes	No/Yes (Typically only one tool)	No
Global Footprint	Yes	No	Yes
Publications	Yes	No	No
Post training support	Yes	No	No
Online Technical Evaluation	Yes	No	No
Customization	Yes	No	No
Online Blogs	Yes	No	No
Extended Hands on	Yes	No	No
Code review	Yes	No	No
Architecture Review	Yes	No	No
Productivity Tools	Yes	No	No
Cost	Low	<Unknown>	Expensive

5. Our Global Footprint

- Headquartered in Bangalore, India
- India
  - Bangalore, Manipal, Cochin, Chennai
  - Pune, Hyderabad
  - Mumbai, Noida
- USA
  - San Jose
  - Boston
  - Austin
- Europe
  - Poland
  - Munich
- Asia-Pac
  - Vietnam
  - Singapore
  - China
  - Taiwan



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6. Other Relevant Courses

- UVM Level 1 (Basic)
- UVM Level 2 (Intermediate)
- UVM Level 3 (Expert)
- UVM RAL
- Art of Debugging with UVM
- ABV-UVM
- Go2UVM
- Graph Based Verification
- Formal Verification

7. Customer list (sub-set)

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8. Course Content

What is UVM?

Universal Verification Methodology (UVM) is the industry standard Verification methodology for Verification using SystemVerilog (SV). UVM provides a mean of doing verification in a well-defined and structured way. It is a culmination of well-known ideas, thoughts and best practices. It is also supported by a standard set of base classes to help building structured verification environment faster. More details about the standard can be found at: http://www.go2uvm.org

What is UVM-RAL?

Register Abstraction Layer is a set of classes that model the memory- mapped behavior of registers and memories in the DUT in order to facilitate stimulus generation and functional checking and optionally some aspects of functional coverage. UVM-RAL is used to create high-level, object-oriented models for memory-mapped registers and memories in a design under verification (DUV). The UVM register layer defines several base classes that, when properly extended, abstract the read/write operations to registers and memories in a DUV. This abstraction mechanism allows the migration of verification environments and tests from block to system levels without any modifications.

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Agenda

Session 1: UVM RAL introduction, RAL Models

- Introduction to UVM
- Register Abstraction Layer – Introduction
- Anatomy of UVM RAL
- Register Models
- Relevant base classes
- Reg Block – container for registers
  - Using build()
  - Using create_map()
  - Using configure()
- Automatic generation of REG models
  - SPI with Registers – An IP Case Study
  - Why Use a Generated Register Model?
- Lab – REG Models

Session 2: Access API

- Register Access API
  - set/update, write
  - get, read, mirror
- Automating RD value checks via mirror()
- Reset value handling
- Lab – REG Access API

Session 3: Integrating with UVC

- Hooking up a UVC with RAL model
  - Developing REG adapter
  - reg2bus(), bus2reg()
- Sequences with UVM_RAL
  - Built-in sequences
  - User written
- Lab – Adapter development
- Lab – SEQ with RAL

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Session 4: Predictor Models

- Predictors in RAL
  - Using Automatic prediction in RAL
- Building custom predictor model
- Lab – RAL Predictors

Session 5: Backdoor accesses in RAL

- Backdoor access in UVM RAL
- Specifying HDL paths
- Mixing FRONT and BACK door

Session 6: RAL Models

- Coverage models in UVM RAL
- Building relevant covergroups
- Using built-in APIs for controlling coverage in RAL
- Using callbacks in RAL
  - Modeling quirky (special) registers
- Case study – safety register block verification with UVM RAL
- Performance considerations in RAL

9. Registration

Send us the following details:

- Name, Email, Contact number of all attendees
- A coordinator name (In case of multiple attendees)
- Training module you are looking for
- Onsite or at CVC premises
- Tentative schedule – month & week (Indicate when your team is available to attend the training)

You may email the details to training@cvcblr.com or

Visit Us: http://www.cvcblr.com or

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Call Us: +91- 42134156, +91-9620209223

+91-9620209223

https://www.linkedin.com/company/cvc-pvt-ltd

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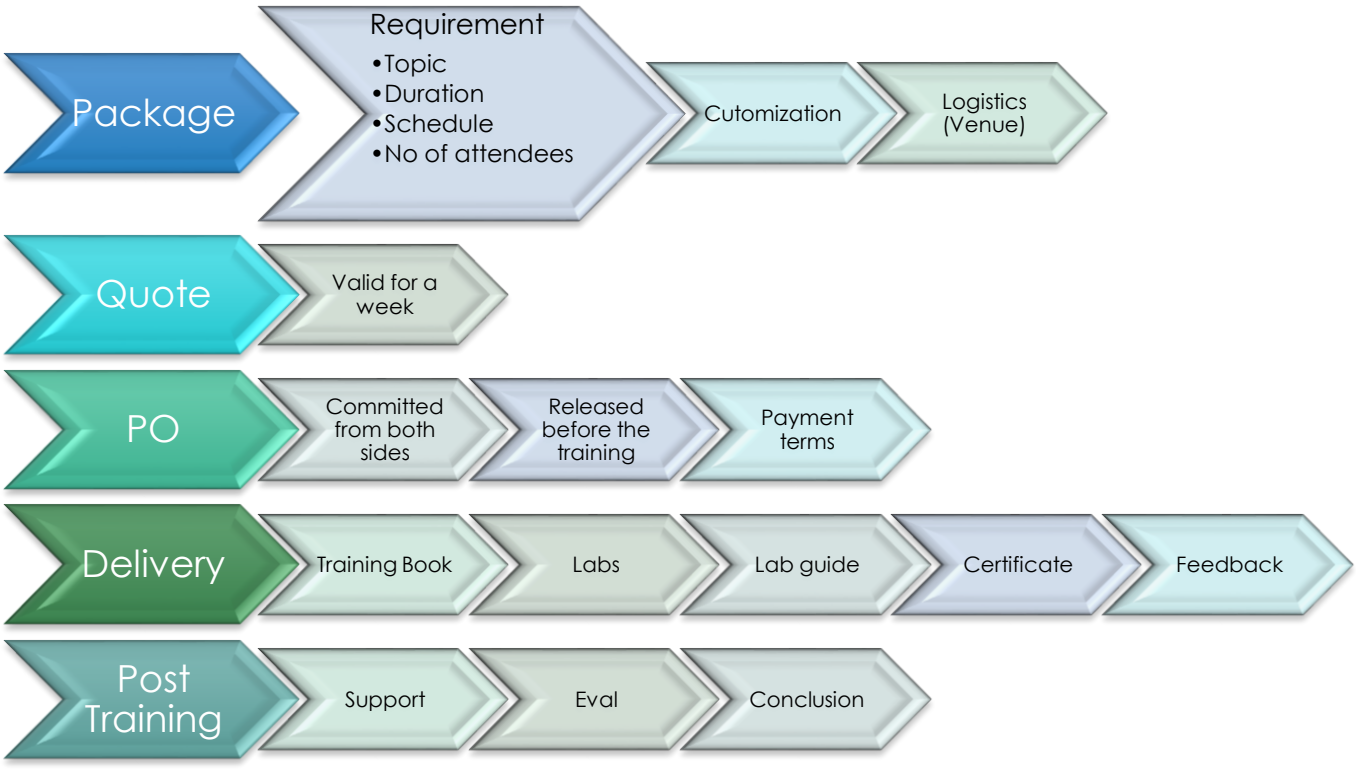
10. Engagement Process



11. More Questions?

Please contact us via email/phone: training@cvcblr.com Call Us: +91- 42134156, +91-9620209223

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