Course Profile

UVM RAL

CVC Pvt. Ltd.

VTD Square, 2nd Floor, 183/3 Sarjapura Road, Dommasandra,
Bangalore – 562125. Ph. No. +91-9620209226
http://www.cvcblr.com, info@cvcblr.com

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Course Profile

1. UVM Register Abstraction Layer (UVM RAL)

CVC's UVM-RAL course gives you an in-depth introduction to the main enhancements that UVM-RAL offers, discussing the benefits and issues with the features and demonstrating how design and verification is more efficient and effective. UVM-RAL training gets the user upto speed with which one can start verifying blocks, IPs, sub-systems and SoCs with large number of configurable registers given a ready-to-use verification environment in UVM.

2. Class Details:

- Duration: 1-day full time
- Prerequisites: Hands-On UVM, Verification, SystemVerilog
- Enrolling for a class: Please refer to Registration section.

3. Trainers Profiles

A. Srinivasan Venkataramanan, CTO

http://www.linkedin.com/in/svenka3

- Over 20+ years of experience in VLSI Design & Verification
- Designed, verified and lead several multi-million ASICs in image processing, networking and communication domain
- Worked at **Philips, Intel,** and **Synopsys** in various capacities. Co-authored leading books in the Verification domain.
- Presented papers, tutorials in various conferences, publications and avenues.
- Conducted workshops and trainings on PSL, SVA, SV, VMM, E, ABV, CDV and OOP for Verification
- Holds M.Tech in VLSI Design from prestigious IIT, Delhi.

B. Ajeetha Kumari, CEO AND MD

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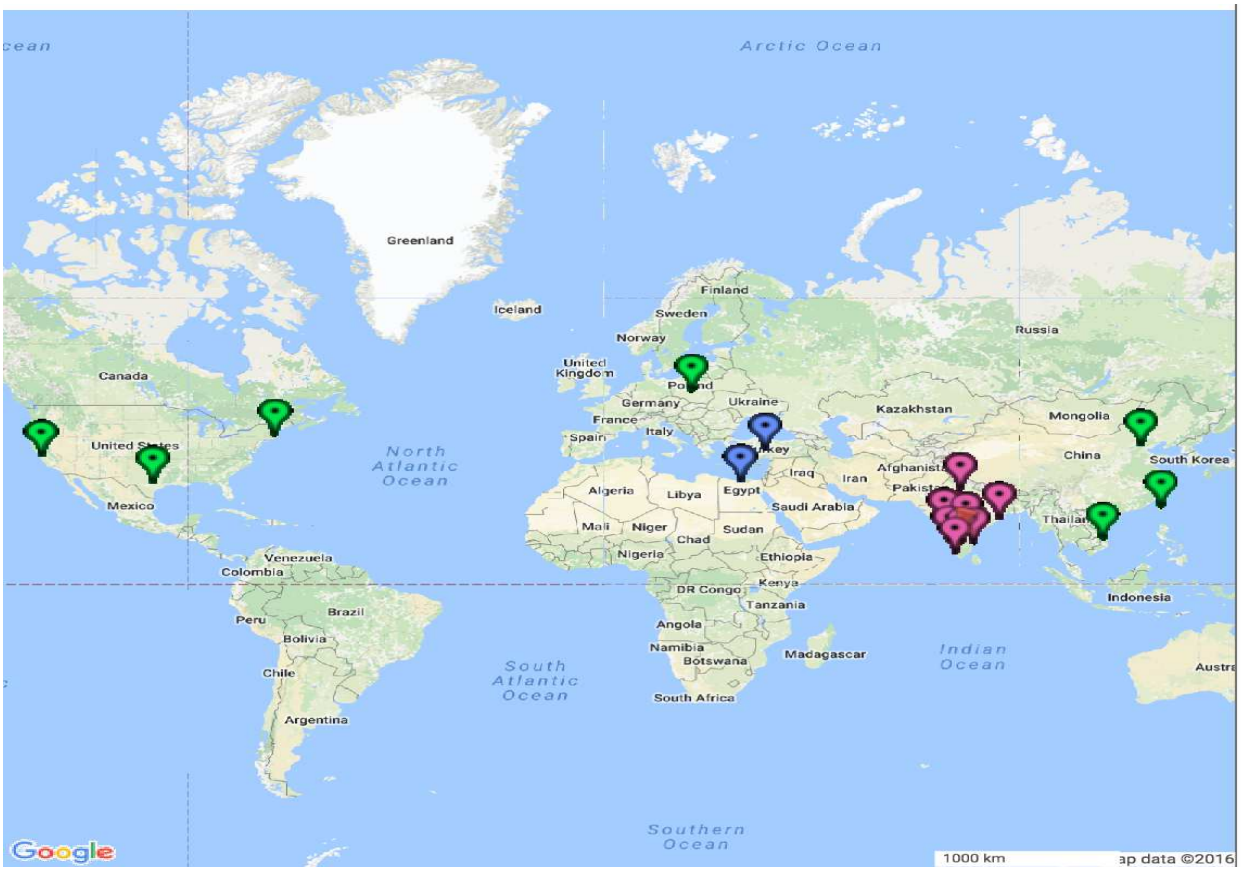
http://www.linkedin.com/in/ajeetha

- Has 18+ years of experience in Verification
- Implemented, architected several verification environments for block & subsystems
- Co-authored leading books in the Verification domain.
- Presented papers, tutorials in various conferences, publications and avenues.
- Has worked with all leading edge simulators and formal verification (Model Checking) tools.
- Conducted workshops and trainings on PSL, SVA, SV, OVM, E, ABV, CDV and OOP for Verification
- Holds M.S.E.E. from prestigious IIT, Madras.

4. Why CVC?

Factor / Vendor	CVC	XYZ training company	EDA Vendor
Training Delivery	World renowned experts	Part timers, in bet'n job engineers	Tool support Engineer
Focus	Verification	Language	EDA tools
Topics covered	User/Verification perspective	Language perspective	Based on the tools strength
How Recently Updated	Last week	Months Back	As old as language was standardized
Verification Expertise	Yes	Depends on the trainer	No
Can I run labs across tools	Yes	Yes	No
Is Content Tool independent	Yes	No/Yes (Typically only one tool)	No
Global Footprint	Yes	No	Yes
Publications	Yes	No	No
Post training support	Yes	No	No
Online Technical Evaluation	Yes	No	No
Customization	Yes	No	No
Online Blogs	Yes	No	No
Extended Hands on	Yes	No	No
Code review	Yes	No	No
Architecture Review	Yes	No	No
Productivity Tools	Yes	No	No
Cost	Low	<Unknown>	Expensive

5. Our Global Footprint



6. Other Relevant Courses

- Art of debugging with UVM
- UVM Level 1
- UVM Level 2
- UVM Level 3
- ABV-UVM
- Go2UVM
- Graph Based Verification
- Formal Verification

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7. Customer set (sub-set)

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8. Course Content

What Is SystemVerilog?

SystemVerilog is a major extension to Verilog-2001, adding significant new features to Verilog for verification, design and synthesis. Enhancements range from simple enhancements to existing constructs, addition of new language constructs to the inclusion of a complete Object-Oriented paradigm features. There are also considerable improvements in the usability of Verilog for RTL design.

What Is UVM?

Universal Verification Methodology (UVM) is the industry standard Verification methodology for Verification using SystemVerilog (SV). UVM provides a mean of doing verification in a well-defined and structured way. It is a culmination of well-known ideas, thoughts and best practices. It is also supported by a standard set of base classes to help building structured verification environment faster. More details about the standard can be found at: http://www.go2uvm.org

What's UVM-RAL?

UVM-RAL is used to create high-level, object-oriented models for memory-mapped registers and memories in a design under verification (DUV). The UVM register layer defines several base classes that, when properly extended, abstract the read/write operations to registers and memories in a DUV. This abstraction mechanism allows the migration of verification environments and tests from block to system levels without any modifications.

Agenda

Session 1: Overview

- Introduction to Register Model Verification in UVM environment

LAB 1 – Simulation of a RAL model

Session 2: Use Model

- Flow for UVM RAL
- Key Components of RAL based verification model

LAB 2 – Important components of a RAL model

Session 3: Constructing a Register Model

- Field Types
- Register Types
- Memory Types
- Block Types
- Packaging a Register Model
- Auto generation of Register models from Specification (EDA tool specific)

LAB 3 – Creating register model

Session 4: Access API

- read/write
- get/set
- randomize
- update
- mirror

LAB 4 – Access API

Session 5: Coverage Models

- Predefined Coverage Identifiers
- Controlling Coverage Model Construction and Sampling

LAB 5 – Coverage model for Registers

Session 6: Integrating a Register Model

- Transaction Adapter
- Writing sequences and tests using RAL models
- Pre-defined sequences

LAB 6 – Integrating a register model

9. Registration

Send us the following details:

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- Name, Email, Contact number of all attendees
- A coordinator name (In case of multiple attendees)
- Training module you are looking for
- Onsite or at CVC premises
- Tentative schedule – month & week (Indicate when your team is available to attend the training)

You may email the details to training@cvcblr.com or

Visit Us: http://www.cvcblr.com or

Call Us: +91-9620209223

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