Course Profile

SystemVerilog Design

CVC Pvt. Ltd.

VTD Square, 2nd Floor, 183/3 Sarjapura Road, Dommasandra,
Bangalore – 562125. Ph. No. +91-9620209226
http://www.cvcblr.com, info@cvcblr.com

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Course Profile

1. SystemVerilog for Design (SVD)

CVC's SystemVerilog for Design course gives you an in-depth introduction to the main enhancements that SystemVerilog offers, discussing the benefits, new features and demonstrating how design is more efficient and effective when using SystemVerilog constructs. It also covers the in-depth details of design constructs of IEEE 1800 standard.

2. Class Details:

- Duration: 3-days full time
- Prerequisites: Design, Simulation, Synthesis and Verilog
- Enrolling for a class: Please refer to Registration section.

3. Trainers Profiles

A. Srinivasan Venkataramanan, CTO

http://www.linkedin.com/in/svenka3

- Over 20+ years of experience in VLSI Design & Verification
- Designed, verified and lead several multi-million ASICs in image processing, networking and communication domain
- Worked at **Philips, Intel,** and **Synopsys** in various capacities. Co-authored leading books in the Verification domain.
- Presented papers, tutorials in various conferences, publications and avenues.
- Conducted workshops and trainings on PSL, SVA, SV, VMM, E, ABV, CDV and OOP for Verification
- Holds M.Tech in VLSI Design from prestigious IIT, Delhi.

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B. Ajeetha Kumari, CEO AND MD

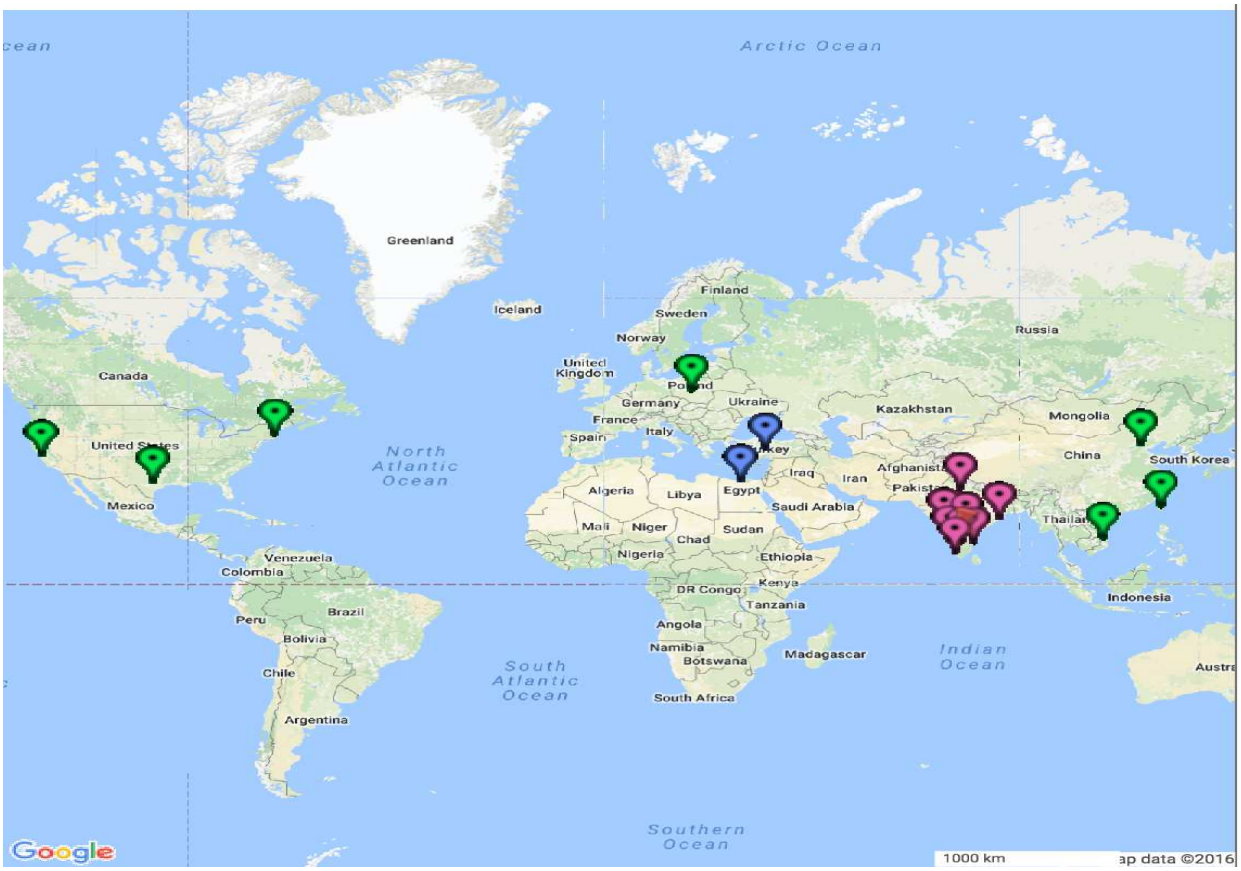
http://www.linkedin.com/in/ajeetha

- Has 18+ years of experience in Verification
- Implemented, architected several verification environments for block & subsystems
- Co-authored leading books in the Verification domain.
- Presented papers, tutorials in various conferences, publications and avenues.
- Has worked with all leading edge simulators and formal verification (Model Checking) tools.
- Conducted workshops and trainings on PSL, SVA, SV, OVM, E, ABV, CDV and OOP for Verification
- Holds M.S.E.E. from prestigious IIT, Madras.

4. Why CVC?

Factor / Vendor	CVC	XYZ training company	EDA Vendor
Training Delivery	World renowned experts	Part timers, in bet'n job engineers	Tool support Engineer
Focus	Verification	Language	EDA tools
Topics covered	User/Verification perspective	Language perspective	Based on the tools strength
How Recently Updated	Last week	Months Back	As old as language was standardized
Verification Expertise	Yes	Depends on the trainer	No
Can I run labs across tools	Yes	Yes	No
Is Content Tool independent	Yes	No/Yes (Typically only one tool)	No
Global Footprint	Yes	No	Yes
Publications	Yes	No	No
Post training support	Yes	No	No
Online Technical Evaluation	Yes	No	No
Customization	Yes	No	No
Online Blogs	Yes	No	No
Extended Hands on	Yes	No	No
Code review	Yes	No	No
Architecture Review	Yes	No	No
Productivity Tools	Yes	No	No
Cost	Low	<Unknown>	Expensive

5. Our Global Footprint



6. Other Relevant Courses

- UVM Level 1 (Basic)
- UVM Level 2 (Intermediate)
- UVM Level 3 (Expert)
- UVM RAL
- Art of Debugging with UVM
- ABV-UVM
- Go2UVM
- Graph Based Verification
- Formal Verification

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7. Customer set (sub-set)

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8. Course Content

What Is SystemVerilog?

SystemVerilog is a major extension to Verilog-2001, adding significant new features to Verilog for verification, design and synthesis. Enhancements range from simple enhancements to existing constructs, addition of new language constructs to the inclusion of a complete Object-Oriented Programming features. There are also considerable improvements in the usability of Verilog for RTL design.

Agenda

DAY1

Session 1: INTRODUCTION

- Introduction to SystemVerilog
- Backward compatibility

Session 2: DATA TYPES

- 4-state & 2-state types
- Casting
  - Static
  - Dynamic
  - Bit stream
- User defined
- Literals
- New data types
  - Void
  - Integer
  - real
- Enumerated types
  - Assignments
  - Methods
  -
- Rules

- Constants
- Strings
- Attribute
- Aggregates
- Enhanced event types
- Scope and lifetime
- Aliasing
- Structures
    - Packed
    - Unpacked
- Unions
    - Packed
    - Unpacked
    - tagged
- LAB 1

Session 3: INTERFACE

- Ports and directions
- Modports
- Clocking block
- Specify
- Tasks and functions
- Parameters
- LAB 2

DAY2

Session 4: PROCEDURE AND PROCESS ENHANCEMENTS

- Always_ff
- Always_comb
- Always_latch
- LAB 3
- Fork … join
    - Any
    - None
    - All
- Process control
- Disable

- Pass by reference
- Import and export function
- Case
  - Unique
  - Priority
- If .. else
  - Unique
  - Priority
- matches
- LAB 4

Session 5: ENHANCED LOOP AND LABELS

- Forever
- Foreach
- Do .. while
- Named blocks
- Final
- Statement labels
- LAB 5

Session 6: NEW OPERATORS AND CONTROL FLOW

- Assignment
- Wild
  - Equality
  - Inequality
- Real
- Size
- Sign
- Overloading
- Conditional
- Inside
- Increment, decrement
- Break
- Continue
- jump
- LAB 6

DAY3

Session 7: ARRAYS AND QUEUES

- Packed
- Unpacked
- Multi-dimensional
- Associative
- Dynamic
- Indexing
- Slicing
- Assignment
- As arguments
- Query functions
- Manipulation methods
- Queue Methods
- LAB 7

Session 8: HIERARCHY

- Packages
- external declarations
- compilation unit
- nested modules
- port connection rules
- time unit and precision
- LAB 8

Session 9: SYSTEM TASKS AND FUNCTIONS, COMPILER DIRECTIVES

- System tasks and functions
    - type name
    - expression size
    - range
    - shortreal conversion
    - array querying function
    - assertion severity
    - assertion control
    - coverage
    - $writememb/h
    - File format
- Compiler directives

- `define
- `include

- Summary, closing remarks
- LAB 9

9. Registration

Send us the following details:

- Name, Email, Contact number of all attendees
- A coordinator name (In case of multiple attendees)
- Training module you are looking for
- Onsite or at CVC premises
- Tentative schedule – month & week (Indicate when your team is available to attend the training)

You may email the details to training@cvcblr.com or

Visit Us: http://www.cvcblr.com or

Call Us: +91-9620209223